CY25701

Programmable High-Frequency Crystal Oscillator with Spread Spectrum (SSXO)

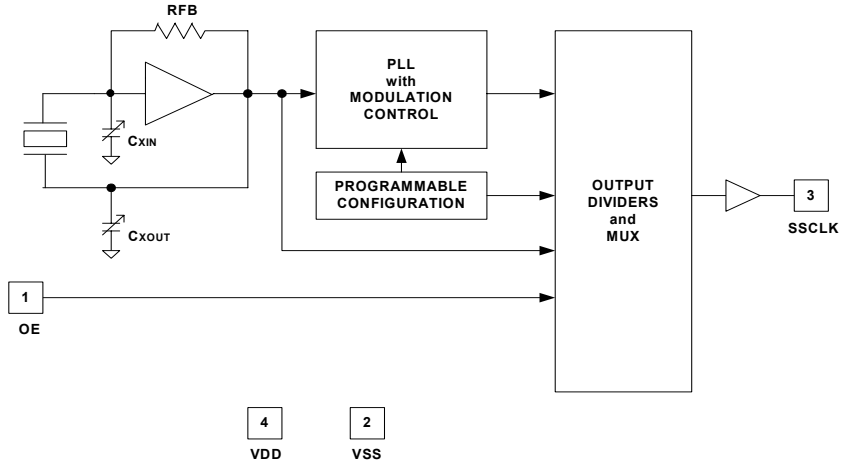
Features

- Crystal Oscillator with Spread Spectrum Clock (SSC)
- Wide operating output (SSCLK) frequency range
- 10–166 MHz
- Programmable spread spectrum with nominal 31.5 kHz modulation frequency
- Center spread: ±0.25% to ±2.0%
- Down spread: –0.5% to –4.0%
- Integrated phase-locked loop (PLL)
- Low cycle-to-cycle Jitter
- 3.3V operation
- Output Enable function
- Package available in 4-Lead Plastic JE SMD

Benefits

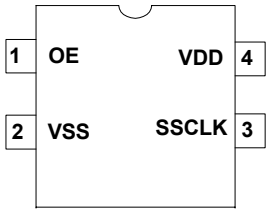
- Provides wide range of spread percentages for maximum electromagnetic interference (EMI) reduction, to meet regulatory agency electromagnetic compliance (EMC) requirements. Reduces development and manufacturing costs and time-to-market.
- Eliminates the need for external crystal oscillator.
- Internal PLL to generate up to 166 MHz output.
- Suitable for most PC, consumer, and networking applications.
- Application compatibility in standard and low-power systems.
- In-house programming of samples and prototype quantities is available using the CY3672 programming kit and CY3613 socket adapter. Production quantities are available through Cypress's value-added distribution partners or by using third-party programmers from BP Microsystems, HiLo Systems, and others.

Logic Block Diagram



Pin Configuration

CY25701
4-pin Plastic SMD



Pin Definition

Pin	Name	Description
1	OE	**Output Enable pin**: **Active HIGH**. If OE = 1, SSCLK is enabled.
2	VSS	**Power supply ground**.
3	SSCLK	**Spread spectrum clock output**.
4	VDD	**3.3V power supply**.

Functional Description

The CY25701 is a Spread Spectrum Crystal Oscillator (SSXO) IC used for the purpose of reducing EMI found in today's high-speed digital electronic systems.

The device uses a Cypress proprietary PLL and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the embedded input crystal. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies are greatly reduced. This reduction in radiated energy can significantly reduce the cost of complying with regulatory agency (EMC) requirements and improve time-to-market without degrading system performance.

The CY25701 uses a programmable configuration memory array to synthesize output frequency and spread%.

The spread% is programmed to either center spread or down spread with various spread percentages. The range for center spread is from ±0.25% to ±2.00%. The range for down spread is from –0.5% to –4.0%. Contact the factory for smaller or larger spread% amounts if required. Refer to *Table 2* for spread selection values.

The frequency modulated SSCLK output can be programmed from 10–166 MHz.

The CY25701 is available in a 4-pin plastic SMD package with operating temperature range of –20 to 70°C.

Table 1. Programming Data Requirement

Pin Function	Output Frequency	Spread Percent Code	Frequency Modulation
Pin Name	SSCLK	SSCLK	SSCLK
Pin#	3	3	3
Units	MHz	%	kHz
Program Value	**ENTER DATA**	**ENTER DATA**	**31.5**

Table 2. Spread Percent Selection

Center Spread	**Code**	**A**	**B**	**C**	**D**	**E**	**F**
	Percentage	±0.25%	±0.5%	±0.75%	±1.0%	±1.5%	±2.0%
Down Spread	**Code**	**G**	**H**	**J**	**K**	**L**	**M**
	Percentage	–0.5%	–1.0%	–1.5%	–2.0%	–3.0%	–4.0%

Programming Description

Field/Factory-Programmable CY25701

Field/Factory programming is available for samples and manufacturing by Cypress and its distributors. All requests must be submitted to the local Cypress Field Application Engineer (FAE) or sales representative. Once the request has been processed, you will receive a new part number, samples, and data sheet with the programmed values. This part number will be used for additional sample requests and production orders.

Additional information on the CY25701 can be obtained from the Cypress web site at www.cypress.com.

Output Frequency, SSCLK Output (SSCLK, pin 3)

The modulated frequency at the SSCLK output is produced by synthesizing the embedded crystal oscillator frequency input. The range of synthesized clock is from 10–166 MHz.

Spread Percentage (SSCLK, pin 3)

The SSCLK spread can be programmed to various spread percentage values from ±0.25% to ±2.0% for Center Spread and from –0.5% to –4.0% for Down Spread. Refer to *Table 2* for available spread options

Frequency Modulation (SSCLK, pin 3)

The frequency modulation is programmed at 31.5 kHz for all SSCLK frequencies from 10 to 166 MHz. Contact the factory if a higher-modulation frequency is required.

Absolute Maximum Rating

Supply Voltage (VDD) ..... –0.5V to +7.0V
DC Input Voltage ..... –0.5V to V_{DD} + 0.5V
Storage Temperature (Non-condensing) .... –55°C to +100°C
Junction Temperature ..... –40°C to +125°C
Data Retention @ Tj = 125°C ..... > 10 years
Package Power Dissipation ..... 350 mW

Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.00	3.30	3.60	V
T_A	Ambient Temperature	–20	–	70	°C
C_{LOAD}	Max. Load Capacitance @ pin 3	–	–	15	pF
F_{SSCLK}	SSCLK output frequency, C_{LOAD} = 15 pF	10	–	166	MHz
F_{MOD}	Spread Spectrum Modulation Frequency	30.0	31.5	33.0	kHz
T_{PU}	Power-up time for VDD to reach minimum specified voltage (power ramp must be monotonic)	0.05	–	500	ms

DC Electrical Characteristics

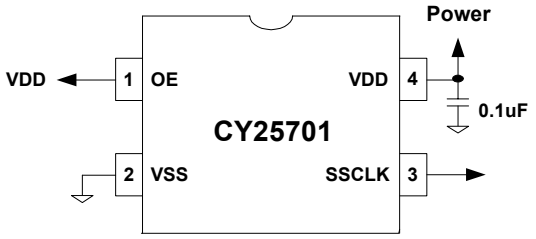
Parameter	Description	Condition	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current (pin 3)	$V_{OH} = V_{DD} – 0.5$, V_{DD} = 3.3V (source)	10	12	–	mA
I_{OL}	Output Low Current (pin 3)	V_{OL} = 0.5, V_{DD}= 3.3V (sink)	10	12	–	mA
V_{IH}	Input High Voltage (pin 1)	CMOS levels, 70% of V_{DD}	$0.7V_{DD}$	–	V_{DD}	V
V_{IL}	Input Low Voltage (pin 1)	CMOS levels, 30% of V_{DD}	–	–	$0.3V_{DD}$	V
I_{IH}	Input High Current (pin 1)	$V_{in} = V_{DD}$	–	–	10	µA
I_{IL}	Input Low Current (pin 1)	$V_{in} = V_{SS}$	–	–	10	µA
I_{OZ}	Output Leakage Current (pin 3)	Three-state output, OE = 0	–10	–	10	µA
C_{IN}[1]	Input Capacitance (pin 1)	Pin 1, or OE	–	5	7	pF
I_{VDD}	Supply Current	V_{DD} = 3.3V, SSCLK = 10 to 166 MHz, C_{LOAD} = 0, OE = V_{DD}	–	–	30	mA

AC Electrical Characteristics[1]

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	SSCLK, Measured at $V_{DD}/2$	45	50	55	%
t_R	Output Rise Time	20%–80% of V_{DD}, C_L = 15pF	–	–	2.7	ns
t_F	Output Fall Time	20%–80% of V_{DD}, C_L = 15pF	–	–	2.7	ns
T_{CCJ1}[2]	Cycle-to-Cycle Jitter SSCLK (Pin 3)	SSCLK ≥133 MHz, Measured at $V_{DD}/2$	–	–	200	ps
		25 MHz ≤ SSCLK <133 MHz, Measured at $V_{DD}/2$	–	–	400	ps
		SSCLK < 25 MHz, Measured at $V_{DD}/2$	–	–	1% of 1/SSCK	s
T_{OE1}	Output Disable Time (pin1 = OE)	Time from falling edge on OE to stopped outputs (Asynchronous)	–	150	350	ns
T_{OE2}	Output Enable Time (pin1 = OE)	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)	–	150	350	ns
T_{LOCK}	PLL Lock Time	Time for SSCLK to reach valid frequency	–	–	10	ms
Δf	Aging in Frequency	T_A = 25°C, First year	–5	–	5	ppm

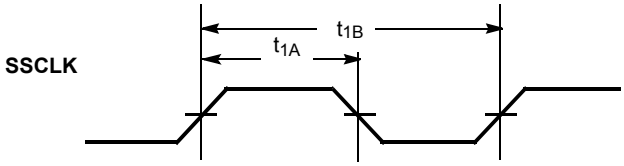
Notes:
1. Guaranteed by characterization, not 100% tested.
2. Jitter is configuration dependent. Actual jitter is dependent on output frequencies, spread percentage, temperature, and output load. For more information, refer to the application note, "Jitter in PLL Based Systems: Causes, Effects, and Solutions" available at http://www.cypress.com/clock/appnotes.html, or contact your local Cypress Field Application Engineer.

Application Circuit

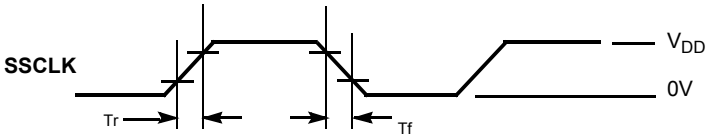


Switching Waveforms

Duty Cycle Timing (DC = t_{1A}/t_{1B})

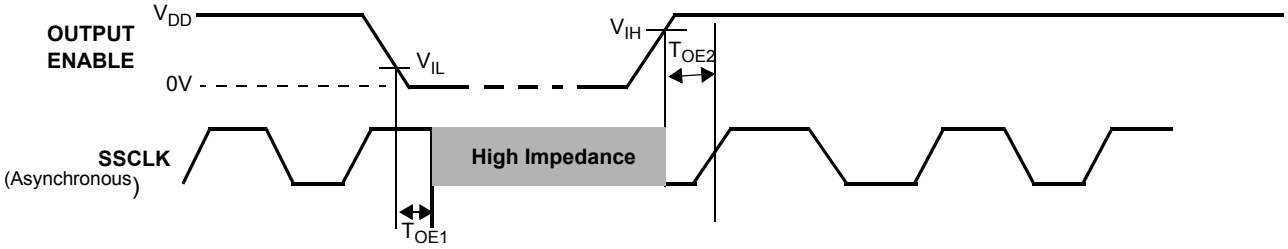


Output Rise/Fall Time

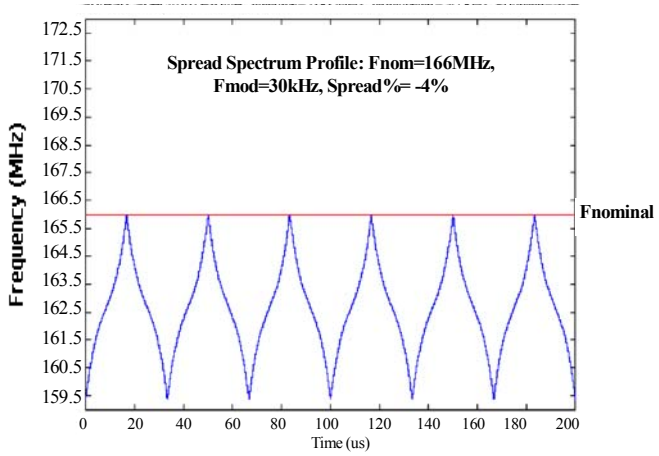


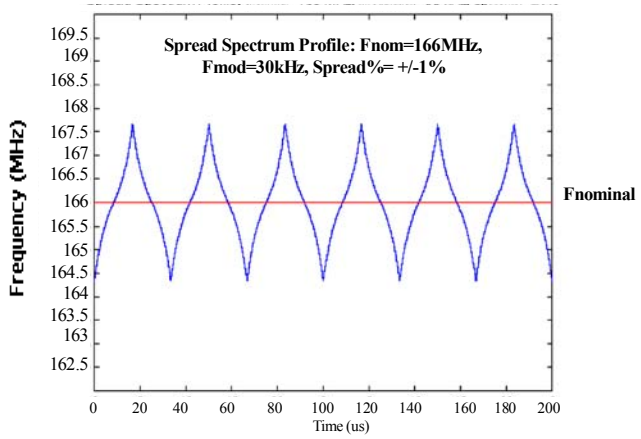
Output Rise time (Tr) = (0.6 x V_{DD})/SR1 (or SR3)
Output Fall time (Tf) = (0.6 x V_{DD})/SR2 (or SR4)
Refer to AC Electrical Characteristics table for SR (Slew Rate) values.

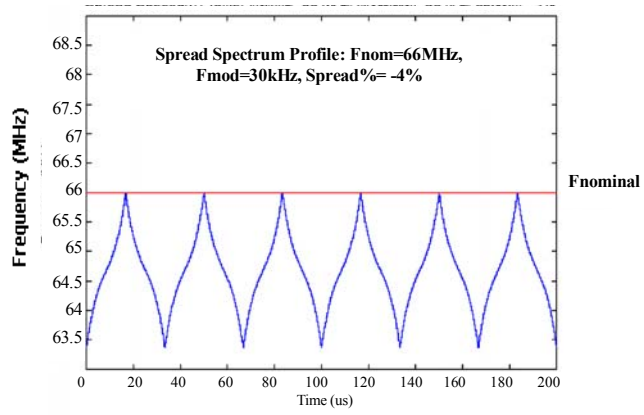
Output Enable/Disable Timing

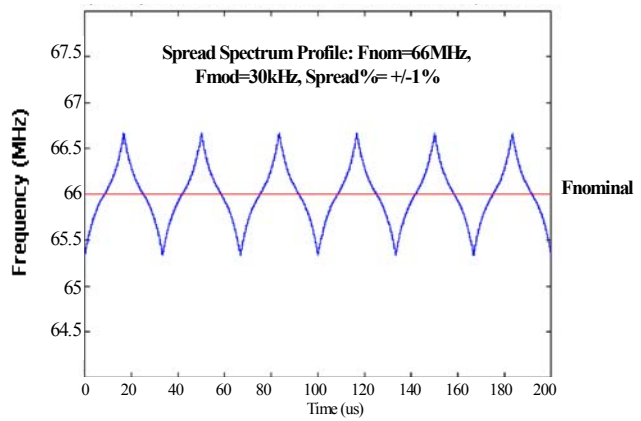


Informational Graphs [3]









Ordering Information

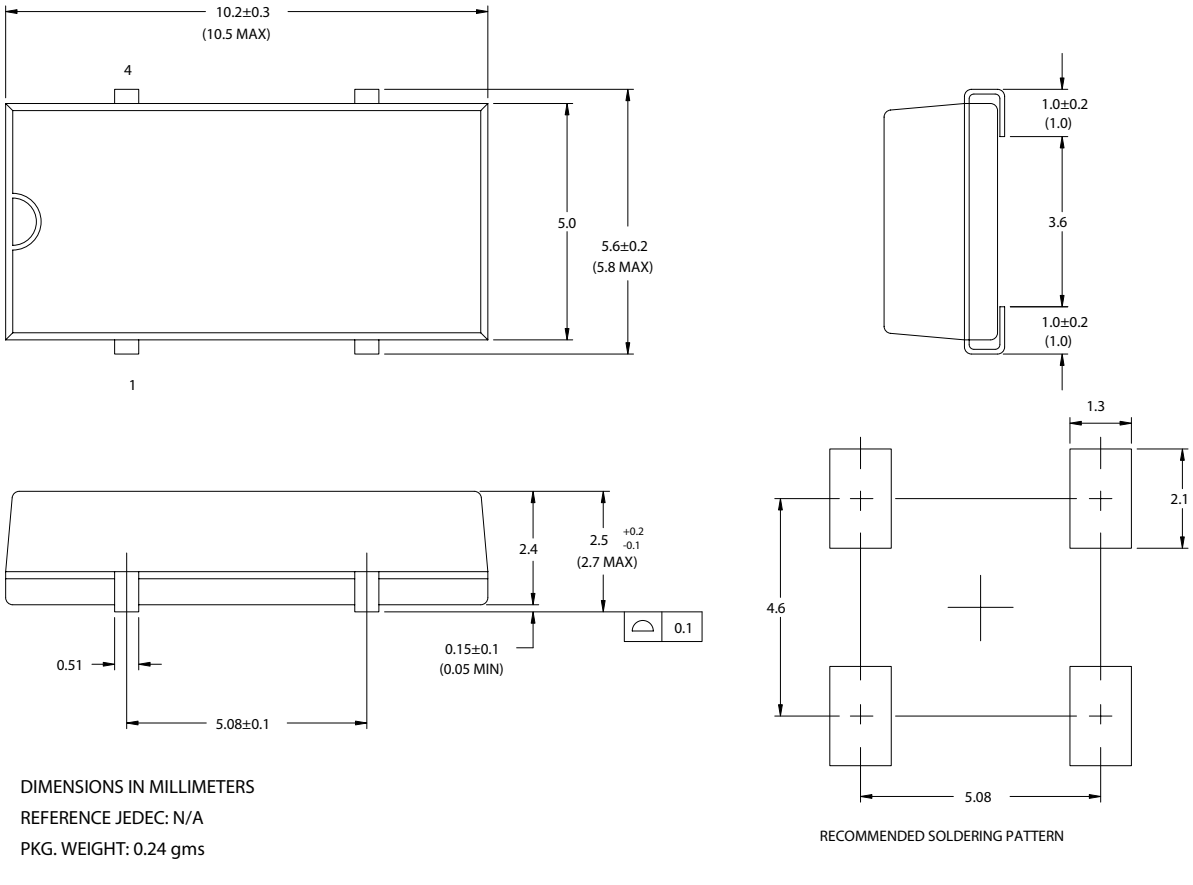
Part Number[4,5]	Package description	Product Flow
CY25701JXCZZZZ	4-Lead Plastic JE SMD – Lead-free	Commercial, –20° to 70°C
CY25701JXCZZZZT	4-Lead Plastic JE SMD, Tape and Reel – Lead-free	Commercial, –20° to 70°C
CY25701FJXC	4-Lead Plastic JE SMD – Lead-free	Commercial, –20° to 70°C
CY25701FJXCT	4-Lead Plastic JE SMD, Tape and Reel – Lead-free	Commercial, –20° to 70°C

Notes:

3. The “Informational Graphs” are meant to convey the typical performance levels. No performance specifications is implied or guaranteed. Refer to the tables on pages 4 and 5 for device specifications.
4. “ZZZZ” denotes the assigned product dash number. This number will be assigned by factory after the output frequency and spread percent programming data is received from the customer.
5. “FJXC” suffix is used for products programmed in field by Cypress distributors.

Package Drawing and Dimension

4-Lead JE04A



DIMENSIONS IN MILLIMETERS

REFERENCE JEDEC: N/A

PKG. WEIGHT: 0.24 gms

RECOMMENDED SOLDERING PATTERN

51-85204-**

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Document History Page

Document Title: CY25701 Programmable High-Frequency Crystal Oscillator with Spread Spectrum (SSXO) Document Number: 38-07684				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	224108	See ECN	RGL	New data sheet
*A	258974	See ECN	RGL	Corrected the product suffix (lead-free) in the ordering information table Added note 4
*B	279379	See ECN	RGL	Added ordering part numbers